Remarks

Brief Summary of the June 17, 2005 Office Action

In the Office Action mailed June 17, 2005, claim 9 was rejected under 35 USC § 112 2nd paragraph as being indefinite. Claims 1-6, 10-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pub. No 2002/0122324 ("Kim et al."). Claims 1, 2, 4, 5, 10, and 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pub. No.2004/0104761 ("Yen"). Claims 13, 14, 16, and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,734,717 ("Min"). Claims 15 and 18 were rejected under 35 U.S.C. § 103 as being unpatentable over Yen in view of Min.

Claims 1-14 and 16-17 remain in the application. Claims 1, 4, 7, 10, 13, and 16 are independent claims and all are currently amended. Claims 15 and 18 have been requested by the Applicants to be cancelled. All of the current amendments to the claims are supported in the original claims, specification, and drawings.

I. Indefiniteness Rejection under §112, 2nd paragraph

Claim 9 was rejected as indefinite because there was no antecedent basis for the limitation "each of said structure." Claim 9 has been amended to remove the reference to "each of said structures" in the preamble of Claim 9.

II. §102(b) Rejection under KIM

Claims 1-6, 7-9, 10-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pub. No 2002/0122324 (KIM).

A. §102(b) Rejection of Independent Claim 1 under KIM:

> Regarding Claim 1, the Examiner stated:
> "As to claim 1, Kim et al. discloses in figure 5 an apparatus for generating a supply voltage internally within an integrated circuit comprising: a charge pump stage structure having a pumping capacitor (CP2) connected to a pumping node (node between PT1 and PT2), a first PMOS device (PT1) connected to an input node, the first PMOS device configured to electrically communicate with the pumping capacitor, wherein the first PMOS device is configured to connect the pumping node to the input node when the pumping capacitor is not boosted; a second PMOS device (PT2) connected to an output node, the second PMOS device configured to electrically communicate with the pumping capacitor, the second PMOS device configured to transfer electrical charge from the pumping node to the output node when the pumping capacitor is boosted, the second PMOS device configured to prevent a reversal current feedback from the output node to the pumping node when the pumping capacitor is not boosted; and a third PMOS device (MPB1) configured to electrically communicate with the first PMOS device, wherein the third PMOS device is configured to connect the pumping node to a gate of the second PMOS device to prevent the current feedback."

Amended Independent Claim 1 claims an apparatus for generating a supply voltage internally within an integrated circuit. The apparatus comprises a charge pump stage structure having a pumping capacitor connected to a pumping node. A first PMOS device is connected between an input node and the pumping node. A second PMOS device is

connected between an output node and the pumping node. The second PMOS device has a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump. A third PMOS device is configured to connect the pumping node to a gate terminal of the first PMOS device to prevent current feedback from the pumping node to the input node.

The Examiner appears to have mischaracterized the KIM reference with respect to amended Claim 1 as having all three of the Applicants' PMOS device. The Kim reference discloses a charge pump circuit having a number of stages, where each stage only has two transistors, such as PT1 and MPB1. Amended Claim 1 of the present application requires three PMOS transistors. The Examiner appears to have supplied the Applicants' claimed second PMOS device of the Applicants' three PMOS transistors by borrowing the PT2 transistor from the next stage of Kim for Kim's first stage. In effect, the Examiner is using the Kim transistors PT1, PT2, PT3, and PT4 as both the Applicants' first PMOS device and simultaneously as Applicants' second PMOS device.

Therefore, the KIM reference has failed to disclose the Applicants' second PMOS device, as claimed in Applicants' amended Claim 1.

Further, the Kim reference does not disclose a second PMOS device that has a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump.

Because one or more essential elements of the Applicants' amended Claim 1 is missing in the Kim reference, amended Claim 1 is not anticipated by the Kim reference.

B. §102(b) Rejection of Independent Claims 4 and 10 under Kim:

Regarding Independent Claims 4 and 10, the Examiner stated:

> "As to claims 4-6 and 10-12, figure 8 shows a symmetrical charge pump having first independent structure (the upper circuit) and second independent structure (the lower circuit), wherein each independent structure has similar configuration as circuit figure 5."

Amended Independent Claim 4 includes a symmetrical charge pump stage structure comprising a first substructure and a second substructure. Each of the substructures has a pumping capacitor connected to a pumping node. A first PMOS device is connected between an input node and the pumping node. Each of the substructures has a second PMOS device connected between an output node and the pumping node, where the second PMOS device has a gate terminal connected to a pumping node of the other substructure. Each of the substructures has a third PMOS device configured to connect the pumping node to a gate terminal of the first PMOS device to prevent reverse current feedback from said pumping node to said input node when the pumping capacitor is boosted.

Amended Independent Claim 10 provides that the third PMOS device has a gate terminal at which is provided a control signal for independently controlling the third PMOS device.

The Examiner appears to have also mischaracterized the KIM reference with respect to the Applicants' amended independent Claims 4 and 10. As mentioned previously in connection with rejection of Claim 1, each stage of KIM is comprised of only two transistors, such as PT1 and MPB1.

Amended Claim 4 and 10 of the present application each require three PMOS transistors. As previously mentioned in connection with rejection of Claim 1, the Examiner appears to have supplied the Applicants' claimed second PMOS device of the Applicants' three PMOS transistors by borrowing the PT2 transistor from the next stage of Kim for Kim's first stage. In effect, the Examiner is using the Kim transistors PT1, PT2, PT3, and PT4 as both the Applicants' first PMOS device and simultaneously as Applicants' second PMOS device. Therefore, the KIM reference has failed to disclose the Applicants' second PMOS device, as claimed in Applicants' amended independent Claims 4, and 10.

Nor does the Kim reference disclose the second PMOS device having a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted.

The Kim reference further does not disclose a third PMOS device that has a gate terminal at which is provided a control signal for independently controlling the third PMOS device.

Because one or more essential element of the Applicants' amended Claim 1 is missing in the Kim reference, amended Claims 4 and 10 are not anticipated by the Kim reference.

C. §102(b) Rejection of Independent Claim 7 under KIM

The Examiner stated: "Claim 7 recites similar limitation of claim 1-3."

Amended Independent Claim 7 is similar to amended independent Claim 1 with the addition of the third PMOS device having a gate terminal at which is provided a control signal for independently controlling the third PMOS device.

As mentioned in connection with the rejection of Claim 1, the Examiner appears to have supplied the Applicants' claimed second PMOS device of the Applicants' three PMOS transistors by borrowing the PT2 transistor from the next stage of Kim for Kim's first stage. In effect, the Examiner is using the Kim's transistors PT1, PT2, PT3, and PT4 as both the Applicants' first PMOS device and simultaneously as Applicants' second PMOS device.

Nor does the Kim reference disclose the second PMOS device having a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted.

Further, the Kim reference does not disclose that the third PMOS device has a gate terminal at which is provided a control signal for independently controlling the third PMOS device.

Because one or more essential elements of the Applicants' amended Claim 7 are missing in the Kim reference, amended Claim 7 is not anticipated by the Kim reference.

III. §102(e) Rejections under YEN

Claims 1, 2, 4, 5, 10, and 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pub. No. 2004/0104761 ("Yen"). The Examiner stated:

> "As to claim 1, Yen discloses in figure 5 an apparatus for generating a supply voltage internally, within an integrated circuit comprising: a charge pump stage structure having a pumping capacitor (540) connected to a pumping node (552), a first PMOS device (506) connected to an input node (VIN), the first PMOS device configured to electrically communicate with the pumping capacitor, wherein the first PMOS device is configured to connect the pumping node to the input node when the pumping capacitor is not boosted; a second PMOS device (566) connected to an output node (590), the second PMOS device configured to electrically communicate with the pumping capacitor, the second PMOS device configured to transfer electrical charge from the pumping node to the output node when the pumping capacitor is boosted, the second PMOS device configured to prevent a reversal current feedback from the output node to the pumping node when the pumping capacitor is not boosted; and a third PMOS device (508) configured to electrically communicate with the first PMOS device, wherein the third PMOS device is configured to connect the pumping node to a gate of the second PMOS device to prevent the current feedback."

Rule 131 Declaration Swearing Behind YEN

The Yen Reference, U.S. Pub. No. 2004/0104761, was cited as an anticipatory reference under 35 U.S.C. § 102(e) for rejection of Claims 1, 2, 4, 5, 10. Note that 37 C.F.R. 1.131 provides that an appropriate declaration may be submitted to establish invention of a rejected claim prior to the effective date of the anticipatory reference on which the rejection is based. The effective date of a U.S. patent application publication is the earlier of its publication date or date that it is effective as a reference under 35 USC § 102(e). Prior invention may be established in a WTO member country.

Two 37 C.F.R. 1.131 Declarations, one signed by the Applicant inventors and the other signed by Patent Attorney Thomas Schneck, are submitted along with the present response to overcome the cited YEN Publication Reference. The Declaration is signed by Jean-Michel Daga and Emmanuel Racape, the named inventors of U.S. Patent Application No. 10/810,033, "High Efficiency, Low Cost, Charge Pump Circuit," filed March 26, 2004 in the U.S. Patent and Trademark Office. A U.S. Patent Application for the Yen Publication Reference was filed in the United States Patent Office on September 24, 2003.

The Applicant inventors' declaration establishes conception of the invention of U.S. Patent Application No. 10/810,033 prior to September 24, 2003, the effective filing date of the Yen Publication Reference.

The Thomas Schneck Declaration establishes diligence in preparing and filing a patent application from just prior to the September 27, 2003 date up to a constructive reduction to practice obtained by the filing of a French Patent Application on December 19, 2003. The present Patent Application claims December 19, 2003 as its effective priority filing date.

Jean-Michel Daga and Emmanuel Racape disclosed the invention in an invention disclosure form submitted to Atmel Corporation's legal department on August 14, 2003, as shown in an attached Exhibit A. A draft patent application concerning the invention was sent to Atmel Corporation by Patent Attorney Thomas Schneck on October 29, 2003. The inventors were submitted a draft application on November 21, 2003. The inventors' comments were received December 4, 2003.

A patent application based on the invention was filed in France (a WTO country) on December 19, 2003. A patent application taking priority from the application filed in France was filed in the United States on March 26, 2004. A copy of the certified copy of the French Filing Receipt is attached as Exhibit D. A copy of the U.S. Utility Patent Application Transmittal letter is attached as Exhibit E. A copy of the U.S. Declaration for a Utility Patent Application claiming a priority date of December 19, 2003 is also attached.

Note that all inventive acts and activities related to actual or constructive reduction to practice related to the invention described in the French and U.S. patent applications took place in France, a WTO country, with the exception of patent drafting activity by Atmel Corporation's legal counsel and patent counsel which took place in the United States,

In conclusion, it is believed that the Declaration shows that the present invention was conceived prior to the effective date of the Yen reference. Jean-Michel Daga and Emmanuel Racape reviewed a copy of a draft patent application initially prepared by October 29, 2003. Comments on a revised draft application were returned to Atmel Corporation on December 4, 2003. Racape reviewed a copy of a revised draft patent application initially prepared by October 29, 2003. A patent application based on the invention was filed in France (a WTO country) on December 19, 2003. The present patent application taking priority from the application filed in

France was subsequently filed in the United States on March 26, 2004.

Consequently, in light of the above discussion, it is believed that the date of invention of the subject matter of the rejected claim was prior to the effective date of the Yen reference.

IV. §102(e) Rejections under MIN

A. §102(e) Rejection of Independent Claim 13 under MIN:

Independent Claim 13 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,734,717 ("Min").

The Examiner stated:

> "As to claim 13, Min's figure 2 shows an apparatus for generating a supply voltage internally within an integrated circuit comprising: a plurality symmetrical charge pump stages (PS1-PS3) cascade-connected in series having: a first symmetrical pump charge stage (PS 1) connected to an input node; and a last symmetrical pump charge stage (PS3) connected to an output node.

Applicants' amended Independent Claim 13 claims an apparatus for generating a supply voltage internally within an integrated circuit. The apparatus comprises a plurality of symmetrical charge pump stages cascade-connected in series and having a first symmetrical pump charge stage connected to an input node and a last symmetrical pump charge stage connected to an output node.

Applicants' amended Independent Claim 13 is amended to include each of said symmetrical pump charge

stages further comprises a first substructure and a second substructure, each of said first and second substructures further comprises:

a pumping capacitor connected to a pumping node;

a first PMOS device connected between an input node and said pumping node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected between an output node and said pumping node; said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted, said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said first PMOS device to prevent the reverse current feedback from said pumping node to said input node when said pumping capacitor is boosted.

The MIN reference discloses a plurality symmetrical charge pump stages (PS1-PS3) cascade-connected in series. However, what the Min reference does not disclose is that each of said symmetrical pump charge stages further comprises a first substructure and a second substructure, each of said first and second substructures further comprises:

a pumping capacitor connected to a pumping node;

a first PMOS device connected between an input node and said pumping node, said first PMOS device configured to electrically communicate with said coupling capacitor, wherein said first PMOS device is configured to connect said pumping node to said input node when said pumping capacitor is not boosted;

a second PMOS device connected between an output node and said pumping node; said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical charge from said pumping node to said output node when said pumping capacitor is boosted, said second PMOS device configured to prevent a reversal current feedback from said output node to said pumping node when said pumping capacitor is not boosted, said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage structure of a symmetrical charge pump, wherein said second PMOS device is configured to prevent reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS

device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said first PMOS device to prevent the reverse current feedback from said pumping node to said input node when said pumping capacitor is boosted.

A number of essential elements of the Applicant's amended claim 13 are missing in the Kim references, such that amended claim 13 is not anticipated by the Kim reference.

B. §102(e) Rejection of Independent Claim 16 under MIN

Regarding Independent Claim 16, the Examiner stated:

"Claim 16 and 17 recite similar limitations of claims 13 and 14. Therefore, they are rejected for the same reasons."

Amended Independent Claim 16 is for an apparatus for generating a supply voltage internally within an integrated circuit. The apparatus comprises:

a symmetrical pump charge stage connected to an input node; and

a plurality of independently controlled symmetrical charge pump stages cascade-connected in series comprising:

a first independently controlled symmetrical pump charge stage connected to said symmetrical pump charge stage; and

a last independently controlled symmetrical pump charge stage connected to an output node;

wherein each of said independently controlled symmetrical charge stages further comprises a first independently controlled substructure and a second

independently controlled substructure, each said independently controlled substructure having:

an input control node;

a pumping capacitor connected to a pumping node;

a first PMOS device connected between said input control node and said pumping node, said first PMOS device configured to electrically communicate with said pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

The apparatus further comprises a second PMOS device connected between an output control node and said pumping node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical current from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent reverse current feedback from said output control node to said pumping node when said pumping capacitor is not boosted; said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage of a symmetrical charge pump, wherein said second PMOS device is configured to prevent a reverse current feedback from said output node to said pumping node when said pumping capacitor is not boosted.

The apparatus also comprises a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said second device to prevent the reversal current feedback from said pumping node to said input control node when said pumping capacitor is boosted; wherein said third PMOS device has a gate terminal at which is provided a control signal for independently controlling said third PMOS device.

The MIN reference discloses a plurality symmetrical charge pump stages (PS1-PS3) cascade-connected in series. However, what the Min reference does not disclose is that:

each of said independently controlled symmetrical charge stages further comprises a first independently controlled substructure and a second independently controlled substructure, each said independently controlled substructure having:

an input control node;

a pumping capacitor connected to a pumping node;

a first PMOS device connected between said input control node and said pumping node, said first PMOS device configured to electrically communicate with said pumping capacitor, wherein said first PMOS device is configured to connect said pumping node to said input control node when said pumping capacitor is not boosted;

a second PMOS device connected between an output control node and said pumping node, said second PMOS device configured to electrically communicate with said pumping capacitor, said second PMOS device configured to transfer electrical current from said pumping node to said output control node when said pumping capacitor is boosted, said second PMOS device configured to prevent reverse current feedback from said output control node to said pumping node when said pumping capacitor is not boosted; said second PMOS device having a gate terminal connected to a pumping node of another charge pump stage of a symmetrical charge pump, wherein said second PMOS device is configured to prevent a reverse current feedback from said

output node to said pumping node when said pumping capacitor is not boosted; and

a third PMOS device configured to electrically communicate with said first PMOS device, wherein said third PMOS device is configured to connect said pumping node to a gate terminal of said second device to prevent the reversal current feedback from said pumping node to said input control node when said pumping capacitor is boosted; wherein said third PMOS device has a gate terminal at which is provided a control signal for independently controlling said third PMOS device.

Because essential elements of the Applicants' amended Claim 16 are missing in the Min reference, amended Claim 16 is not anticipated by the Min reference.

V. § 103 Rejection of Claims 15 and 18 under YEN in view of MIN

Claims 15 and 18 were rejected under § 103 as being unpatentable over Yen in view of Min. Claims 15 and 18 have been cancelled and their subject matter is now included in amended independent Claim 13 and 15.

Summary

Applicants have amended claims 1-14, and 16 and 17. Claims 15 and 18 have been cancelled. The independent claims are believed to be in condition for allowance and such action is requested. Being dependent upon allowable independent claims, the remaining dependent claims are also believed to be in condition for allowance and such action is requested.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: Sally Azevedo
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Respectfully submitted,

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